

A Comparative Study of Shift Register Using Flip-Flops and Latches

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ABSTRACT: This paper mention the comparative study of shift register using flip-flops and latches. Flip-flop and latches are the basic building blocks in VLSI circuits. Here consider the shift register with latches and flip-flops. Latches are smallest circuit of flip-flops, so to reduce area and power, flip-flops are replaced by latches. In the literature study of several methods of shift register based on latches are compared in this paper. Based on the result a accurate method is to consume less the area and power is that the shift register is build with multiple non overlap delayed clock pulsed latches. To avoid the timing problem in shift register by using latches instead of flip-flop, multiple non overlap delayed pulsed clock is applied to the latches. The ordinary 2:4 decoder is enables each latches. This is a efficient method for low power and area efficient shift register in VLSI circuits.

KEYWORDS: Decoder, Flip-flops, VLSI, pulsed latches, Shift registers.

I. INTRODUCTION

The power and area are the important constrain in the VLSI circuit technology. This technology world needs a low power and area efficient circuit design for the digital system applications. Shift registers are very important in VLSI design because it is the basic building block in many VLSI circuits such as communication receivers[1], image processing ICs[2], displays and digital filters[3]. In application take an example, the demand for high quality image data increased so the size of image data is also increased because of this the word length of the shift register must be large to process large image data in image processing ICs. An N bit shift register is compose of N bit D flip-flops. As the word length of the shift register increases, the area and power consumption of the shift register also increases so it becomes an important design consideration.

Flip flop and latches can store a single bit of binary data i.e. 1 or 0. If it needs to store many bits of data, need multiple flip-flops or latches. As a single flip-flop is used to store one bit, then n flip-flops are connected in an order to store n bits of data. In digital electronics, a register is a device which is used to store the information. Flip-flops are used in constructing registers. But it takes a large power and area, to reduce the power and area the large flip-flops are replaced by small flip-flops that are the pulsed latches [4]. The timing problem of pulsed latches is solved by using multiple non overlap delayed circuit [4]. The comparative study of shift register based on flip-flops, latches, pulsed latches and decoder enabled pulsed latches are mentioned in this paper.

The rest of the paper is organized as follows: Section II Shift register using latches, Section III proposed shift register, Section IV Result and Discussion, finally the section V shows the Conclusion of the work.

II. SHIFT REGISTER USING LATCHES

Latches and flip-flops are the building blocks of sequential circuits and these can be built from logic gates, and latches are simple and small size circuit. Flip-flop and latch can store one bit of data at a time. The main difference between the latches and flip-flops is that, a latch checks input continually and change the output whenever there is a change in input.

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But, flip-flop is a combination of latch and clock that continuously checks input and changes the output time adjusted by the clock. Conventional Shift registers built using flip-flops are take more power and area.

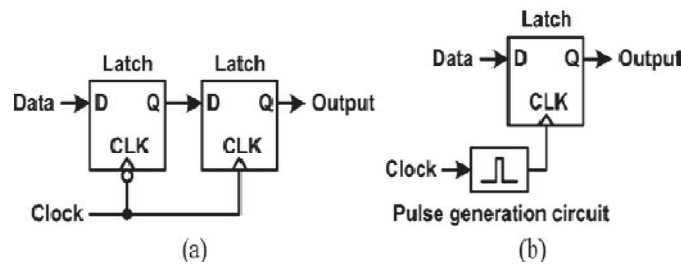


Fig. 1 (a) Master-slave flip-flop. (b) Pulsed latch.[7]

The flip-flops are cascaded to form the shift register which shares the same clock, the output of each flip-flop data is given to next flip-flop. A master-slave flip-flop using two latches shown in Fig. 1(a), it can be replaced by a pulsed latch with a latch and a pulsed clock signal is shown in Fig. 1(b)[7]. All pulsed latches are share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. From this the pulsed latch is an attractive solution for small area and low power consumption is understood. Using pulsed latches there occurs timing problem is shown in fig.2. Arrangement of such circuit is shown in fig.2 (a) and result wave form is shown in fig.2 (b). The operational wave form shows the timing problem between latches in shift register. The output signal of the first latch (Q_1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width (T_{pulse}) But the second latch has an uncertain output signal (Q_2) because its input signal (Q_1) changes during the clock pulse width.

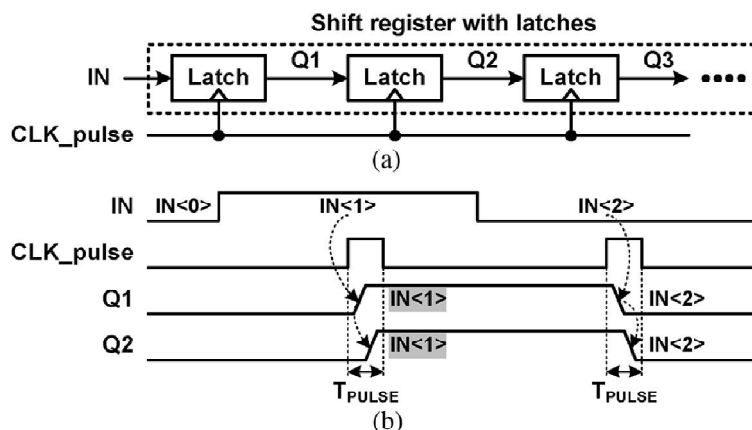


Fig. 2 Shift register with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms

To solve this timing problem there are several methods[4].

Method I: one of the solution to solve the timing problem is to add a delay circuit between each latches. Fig.3 (a) shows such arrangement and fig.3 (b) corresponding result wave form and from the wave form Q_1 and Q_2 are change in the T_{pulse} duration.

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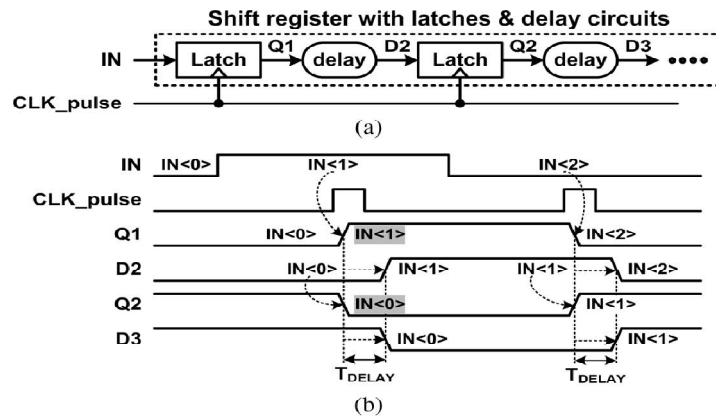


Fig. 3 Shift register with latches, delay circuits, and a pulsed clock signal. (a) Schematic. (b) Waveforms.

Method II: Another solution is to add delay in clock signal, ie. Multiple non overlap delayed pulsed clock is used to enables each latch. Fig.4 (a) shows the architecture and (b) is the output wave form. From this wave form it is understood that the timing problem is eliminated.

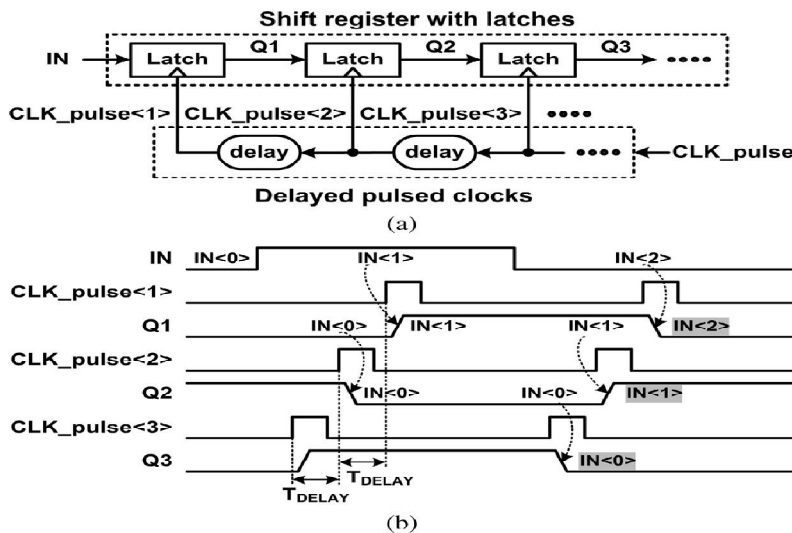


Fig. 4 Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms.

But the method I and method II solves the timing problem but take more power and area because of the delay circuits. Here the number of delay circuit is large.

Method III : Byung-Do Yang introduce a shift register based on delayed pulsed latches are mentioned in [4] can reduce power and area. The arrangement of such method is shown in fig.5(a) and corresponding wave form fig.5(b).

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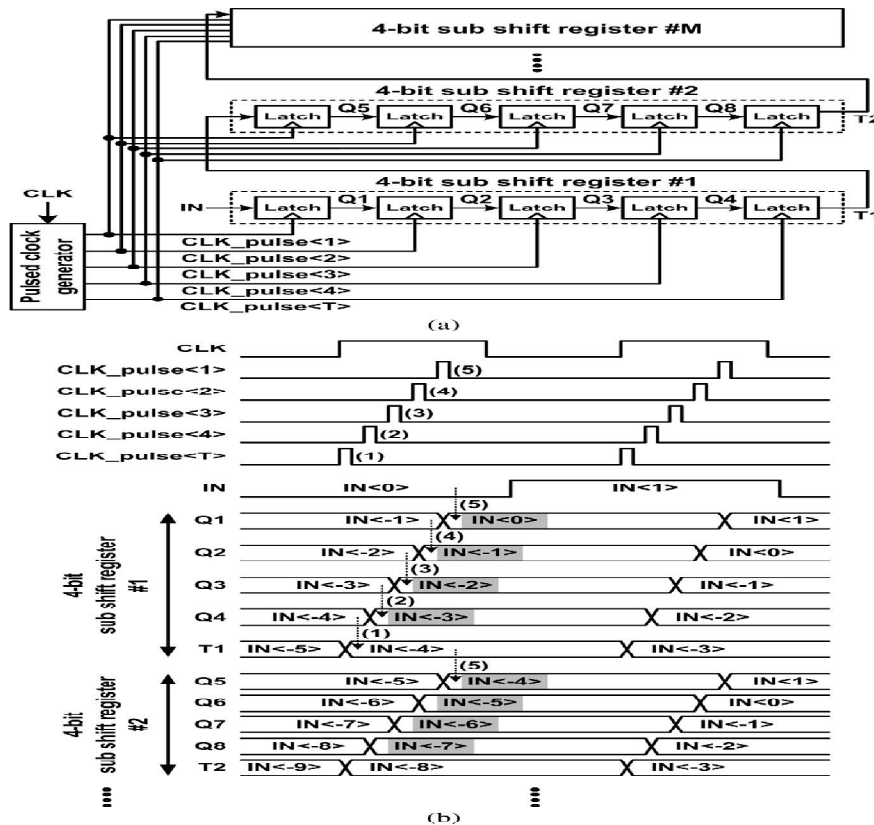


Fig.5 shift register. (a) Schematic. (b) Waveforms[4]

In this method the m bit shift register is divided in to 4 bit sub-shift register and each sub shift register consist of 5 latches from this one latches are used for temporary storage. And the clock pulse generator is used to enable the pulsed clock signal. Pulsed clock generator has 5 clock pulse circuit and each clock pulse circuit consist of a delay circuit, two inverter, a AND gate and a buffer. This method is better than the previous method. But it also use more area for temporary storage latches and pulsed clock generator circuit.

III PROPOSED SHIFT REGISTER

Fig.6 shows the architecture of proposed shift register using decoder enabled pulsed latch. Here an example of 16bit shift register split into 4 sub shift registers and each sub shift register has 4 latches. in proposed method eliminate the temporary storage latches and modified the pulsed clock generator circuit as shown in fig.7. the output from the decoder will avoid the data loss so the temporary storage is not required because of the pulse duration of the pulsed clock generator are modified using 2:4 decoder. The Input signal (IN) is applied to the first latch in the first sub shift register and the output are mentioned as Q₁-Q₁₆.

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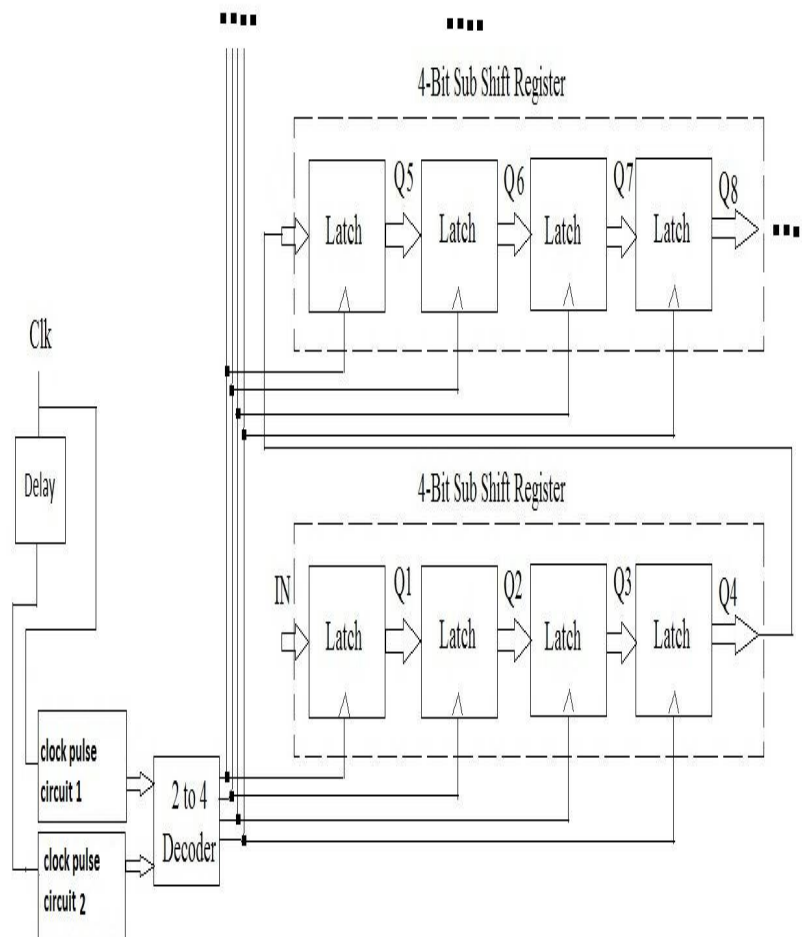


Fig. 6 proposed shift register using decoder enabled pulsed latch

In this arrangement reduces the number of delay circuits by substituting a delayed clock pulse generator using decoder. General 2:4 decoder is used for this proposed shift register as clock signal. Two clock pulse circuit are used where the main clock is applied directly clock pulse circuit 1 and connected after a delay to the clock pulse circuit 2. Clock pulse circuit consist of a delay, inverter and a AND gate, then output of the clock pulse circuit is connected to 2:4 decoder and get the output D_3, D_2, D_1 and D_0 .

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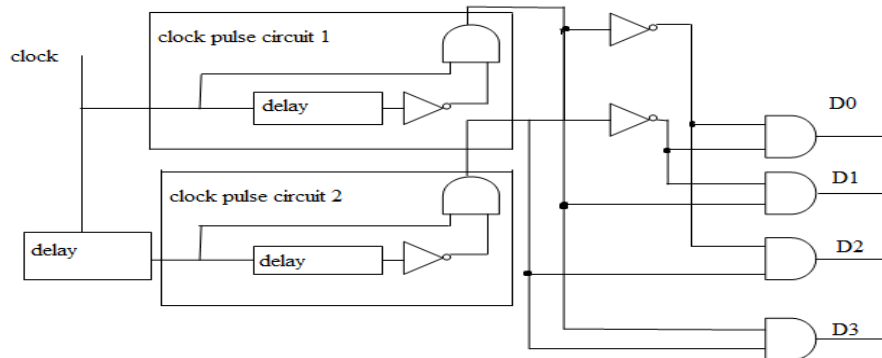


Fig.7 Delayed clock pulse generator using decoder

A binary decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. It will convert binary information from n input signals to as many as 2^n unique output signals. In this application a decoder has 2 input and 4 outputs that combination is shown in table 1.

Table 1: Truth table of decoder

Input combination		D ₀	D ₁	D ₂	D ₃
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

A_0 and A_1 are inputs And D_0 - D_3 are outputs, both inputs are 0 then get D_0 as high, A_0 is 0 and A_1 is 1 then D_1 is high, A_0 is 1 and A_1 is 0 then D_2 is high and both inputs are 1 then get D_3 is high. These output are act as delayed clock pulse for the proposed shift register. The input of decoder, A_0 and A_1 signals are generated by the clock pulse circuits from the main clock.

IV. RESULT AND DISCUSSION

The power analysis and area calculation are done using Xilinx software. Area is calculated according to the number of gates and power in mW. Table 2 shows the comparison of shift register with flip-flops and latches. Spartan 2E family is consider for the experiment. Power and area are slightly varies with FPGA family.

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Table 2 Power and Area comparison.

parameter	Shift register with flip-flops	Shift register with pulsed latches	Proposed shift register
Power(mW)	134	124	104
Area(gate count)	136	32	30

From the comparison table 2, the proposed shift register based on decoder enabled pulsed latch can save more power and area than conventional shift register using flip-flops. The shift register based on latches are more suitable for low power VLSI applications and it also reduces the chip size.

V. CONCLUSION

From the analysis the shift register with latches can reduce the area and power. The proposed 16-bit shift register consumes more the power and area than the conventional shift register using flip-flops and other methods with latches. The proposed shift register is constructed using pulsed latches, each latches are enabled using decoder. Here the 16 bit shift register is divided into 4 bit sub shift registers and the main clock is changed to delayed non-overlap multiple pulses that can solve the timing problem in the latches. The delayed clock pulses are generated using two clock pulse circuit and a 2:4 decoder it can reduce area and power more efficiently. This type of arrangement is less complex and simple than other conventional methods. It can save more power and area compared conventional shift registers used by flip-flops and other pulsed latches methods.

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